REMARKS / ARGUMENTS

Claims 1-17 remain in the application, all of which stand rejected.

1. Provisional Double Patenting Rejection

Claims 1, 3-7, 12 and 17 stand provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-6 and 10-13 of copending U.S. Patent Application No. 10/666,024.

In Item 1 on page 2 of the Office Action dated July 31, 2006 for the instant application, the Examiner states (italicized emphasis added), in part:

> A rejection based on double patent of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process... may obtain a patent therefore ..." (Emphasis added). Thus, ***the term "same invention," in this context, means an invention drawn to identical subject matter.***
>
> ***A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope.*** The filing of a terminal disclaimer cannot over come a double patenting rejection based upon 35 U.S.C. 101.

Applicants believe that the rejection of claims 1, 3-7, 12 and 17 under 35 U.S.C. 101 is improper at least for the reason that claims 1, 3-7, 12 and 17 are not coextensive in scope with claims 1-6 and 10-13 of copending U.S. Patent Application No. 10/666,024. Applicants respectfully request withdrawal of this rejection.

In addition, in Item 2 on page 2 of the Office Action dated July 31, 2006 for the instant application, the Examiner states (italicized emphasis added), in part:

...the examiner user [*sic*; used] rationale reasoned from legal precedent that an omission of an element with the consequent loss of its function is deemed ***obvious***.

In copending U.S. Patent Application No. 10/666,024, in Item 2, page 2 of the Office Action dated 01/24/2006, the Examiner states, in part:

> Claims 1-6 and 10-13 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 2-7, 13 and 17 of copending Application No. 10/681,068 [i.e., the instant application]. Although the conflicting claims are not identical, they are not patentably distinct from each other because all of the limitations of the rejected claims are claimed in at least one of the claims 1, 3-7, 13 and 17 of applicant's copending application, and there is no reason why the rejected claims could no [*sic*; not] have been presented in the copending application 10/681,068 [i.e., the instant application].

In copending U.S. Patent Application No. 10/666,024, in Item 2, page 3 of the Office Action dated 07/13/2006, the Examiner states:

> 2. Claims 1-6 and 10-13 are [*sic*] remain provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 37 [*sic*; 3-7], 13 and 17 of copending application No. 10/681,068 [i.e., the instant application]. (See the office action dated on 1/24/06).

If the Examiner believes that claims 1, 3-7, 12 and 17 should be provisionally rejected on the grounds of a nonstatutory obviousness-type double patenting over claims 1-6 and 10-13 of copending U.S. Patent Application No. 10/666,024, Applicants will file a Terminal Disclaimer if and when U.S. Patent Application No. 10/666,024 matures into a patent.

2. Rejection of Claims 1-17 Under 35 U.S.C. 112, First Paragraph

Claims 1-20 stand rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement.

In Item 4 on page 3 of the Office Action dated July 31, 2006 for the instant application, the Examiner states, in part:

> The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. This disclosure fails to state or teach one of ordinary skill in the art how billing predictor 104 "uses the required memory to estimate a cost to execute the test vectors". No working examples disclosing the necessary operation have been provided. Without this disclosure, one skilled in the art cannot practice the invention without undue experimentation because of unknown operation of the billing predictor. Since claims 2-7 are dependent on claim 1, claims 9-12 are dependent on claim 8 & claims 14-17 are dependent on claim 13[,] these claims are also rejected.

Applicants respectfully disagree. The specification of the instant application provides examples of the operation of billing predictor 104. Examples are provided in paragraph [0017] as follows:

> [0017] Billing predictor 104 may use the required memory determined 205 by logic 102 to estimate a cost to execute the test vectors. The cost may be estimated by using a billing rate and billing scheme charged for the use of various amounts of memory. The billing rate/scheme may correlate to rates charged by a supplier of test services or may be rates charged to use memory of a tester. Additional factors, such as speed requirements, may also be taken into account when estimating the cost.

The specification of the instant application provides further examples of the operation of billing predictor 104 in paragraphs [0023] and [0024] as follows:

> [0023] The billing predictor 104 may use various billing rates and schemes that correlate to the configuration of the tester to estimate the cost required to execute the tests. By way of example, in a per pin configuration, billing predictor may use a rate charged for memory to calculate costs to use the required memory for each pin and then total the costs. Correspondingly different calculations may be made for different test environments, such as one memory for tester, or configuration in

which all pins on a board are given the same amount of memory but memory can vary between boards.

[0024] The cost estimated 205 by billing predictor 104 may then be displayed to a user. Additional information, such as the test requiring the most memory, may also be provided. The user may use this information to find the lowest cost supplier of test services and/or to reconfigure their tests to meet a test budget.

Accordingly, claims 1-17 are believed to be allowable.

3. Rejection of Claims 1-17 Under 35 U.S.C. 112, Second Paragraph

Claims 1-17 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 8 and 13

In Item 6 on page 3 of the Office Action dated July 31, 2006, the Examiner states, in part:

> When referring to independent claims 1, 8 & 13, the examiner is unclear as to how the required memory is determined. The applicant uses this claim terminology: "determining a required memory needed to execute the plurality of test vectors."

For claims 1 and 13, the limitation of "determining a required memory needed to execute the plurality of test vectors" is clearly defined by the claims, and is described in the specification of the instant application. For claim 8, the limitation of "logic...to determine a required memory needed to execute the plurality of test vectors" is clearly defined by the claim, and is described in the specification of the instant application. See, for example, paragraphs [0014] through [0016] (italicized emphasis added) as follows:

> [0014] As shown in FIG. 2, logic 102 may be used to read 200 a test file containing one or more tests to be performed on a device, such as a system-on-a-chip (SOC). Each of the tests may include a plurality of test vectors to be applied to the device under test. Logic 102 may then ***determine 205 a required memory needed to execute the plurality of***

> ***test vectors. By way of example, the number of test vectors for each test in the test file may be counted and the required memory may be determined to be equal to the number of test vectors required for the test with the highest number of test vectors.***
> [0015] The determination of the required memory may vary depending upon the configuration of the tester. In one embodiment, the tester that is used to test the device may include a plurality of boards. Each board may include a plurality of pins that may be used to drive inputs and receive outputs from the device under test. Each pin may include its own memory to use during the testing of the device. The memory may be used to store pin specific vector information. In alternate embodiments, memory may not be included on each pin, but may instead be included for each board or other component of the tester, or pooled in a central location and dynamically allocated by a centralized test processor.
> [0016] In one embodiment, ***logic 102 may determine 205 an amount of pooled memory required for the tester to execute the test vectors***. In another embodiment, a required memory needed for each board of a tester to execute the test vectors for the board may be determined. By way of example, ***in embodiments having a memory associated with each pin, a required memory needed for each board may be determined by determining the memory requirements for the pin with the highest memory usage***. In a third embodiment, ***logic 102 may determine 205 the required memory needed for each pin to execute the vectors for the pin***. Appropriate determinations 205 for other configurations are also contemplated.

Furthermore, the specification of the instant application describes the limitations of "determining a required memory needed to execute the plurality of test vectors" and "logic...to determine a required memory needed to execute the plurality of test vectors" in paragraphs [0018] through [0021] (italicized emphasis added) as follows:

> [0018] FIG. 3 illustrates an exemplary embodiment of a method for determining 205 a required memory that may be used by logic 102. The method begins by determining 305 a first memory requirement for a first pin to execute the test vectors for a first test in the test file. By way of example, ***the first memory requirement may be determined 305 by counting the number of test vectors in the first test for the first pin. The required memory is then set 310 to be equal to the first memory requirement.***
> [0019] Another pin of the tester having test vectors in the first test is selected and a second memory requirement for the selected pin to execute the test vectors for the first test is determined 315. ***The second memory requirement may be determined 315 by counting the number of test vectors in the first test for the selected pin. If the second***

> ***memory requirement exceeds the current value of the required memory 320, the required memory is set 325 equal to the second memory requirement.***
> [0020] After 325, or if the second memory requirement does not exceed the current value of the required memory 320, a determination is made as to whether there are more pins 330 having test vectors in the first test to process. If there are more pins, processing continues back at 315 for the next pin. Otherwise, a determination is made as to whether there are more tests in the test file 335.
> [0021] If there are more tests, 315-330 are repeated for the next test for each pin having test vectors to execute for the test. After all the tests have been processed, the method ends 340. Thus, it should be appreciated that at the conclusion of the method the required memory is determined to be equal to the memory requirements for the test and pin combination with the highest memory requirements.

The specification of the instant application also describes the limitations of "determining a required memory needed to execute the plurality of test vectors" and "logic...to determine a required memory needed to execute the plurality of test vectors" in paragraphs [0018] through [0021] (italicized emphasis added) as follows:

> [0022] In alternate embodiments, the required memory may be determined in a manner different from that shown in FIG. 3. The determination 205 may depend upon how available memory is allocated in the tester. For example, in one embodiment, the memory available for a pin may depend on the board where the pin is located. Pins on one board may have the same amount of memory available as other pins on the same board, while the amount of memory available for pins may vary between boards. In this embodiment, ***a required memory may be calculated for each board by determining the memory requirements for the test and pin combination with the highest memory requirements for each board using a method similar to that described in FIG. 3.*** In a second embodiment, memory may be allocated on a per pin basis. In this embodiment, ***a required memory may be determined for each pin.*** Other exemplary embodiments, such as embodiments with one memory available for all the pins of a board, may use corresponding different calculations.

Accordingly, Applicants believe that the limitation of "determining a required memory needed to execute the plurality of test vectors" is clearly defined and claims 1 and 13 are allowable. Applicants believe that the limitation

of "logic...to determine a required memory needed to execute the plurality of test vectors" is clearly defined and claim 8 is allowable.

In Item 6 on pages 3-4 of the Office Action dated July 31, 2006 for the instant application, the Examiner states, in part:

> The examiner is also unclear as to how the cost will be estimated. The applicant states within the Specification that different calculations can be used, but does not state any of the methods as to how the cost will be calculated. The applicant uses this claim terminology: "using the required memory to estimate a cost to execute the test vectors".

Applicants respectfully disagree. For claims 1 and 13, the limitation of "using the required memory to estimate a cost to execute the test vectors" is clearly defined by the claims, and is described in the specification of the instant application. For claim 8, the limitation of "a billing predictor, communicatively coupled to the logic, to use the required memory to estimate a cost to execute the test vectors" is clearly defined by the claim, and is described in the specification of the instant application. See, for example, paragraph [0017] (italicized emphasis added) as follows:

> [0017] Billing predictor 104 may use the required memory determined 205 by logic 102 to estimate a cost to execute the test vectors. The cost may be estimated ***by using a billing rate and billing scheme charged for the use of various amounts of memory.*** The billing rate/scheme may correlate to rates charged by a supplier of test services or may be rates charged to use memory of a tester. Additional factors, such as speed requirements, may also be taken into account when estimating the cost.

Furthermore, the specification of the instant application describes the limitations of "determining a required memory needed to execute the plurality of test vectors" and "a billing predictor, communicatively coupled to the logic, to use the required memory to estimate a cost to execute the test vectors" in paragraphs [0023] and [0024] (italicized emphasis added) as follows:

> [0023] The billing predictor 104 may use various billing rates and schemes that correlate to the configuration of the tester to estimate the cost required to execute the tests. ***By way of example, in a per pin configuration, billing predictor may use a rate charged for memory to***

> ***calculate costs to use the required memory for each pin and then total the costs.*** Correspondingly different calculations may be made for different test environments, such as one memory for tester, or configuration in which all pins on a board are given the same amount of memory but memory can vary between boards.
> [0024] The cost estimated 205 by billing predictor 104 may then be displayed to a user. Additional information, such as the test requiring the most memory, may also be provided. The user may use this information to find the lowest cost supplier of test services and/or to reconfigure their tests to meet a test budget.

Accordingly, Applicants believe that the limitation of "using the required memory to estimate a cost to execute the test vectors" is clearly defined and claims 1 and 13 are allowable. Applicants believe that the limitation of "a billing predictor, communicatively coupled to the logic, to use the required memory to estimate a cost to execute the test vectors" is clearly defined and claim 8 is allowable.

Claims 2-7

Claims 2-7, which each depend either directly or ultimately from independent claim 1, are believed to be allowable for at least the above-identified reasons.

Claims 9-12

Claims 9-12, which each depend directly from independent claim 8, are believed to be allowable for at least the above-identified reasons.

Claims 14-17

Claims 14-17, which each depend directly from independent claim 13, are believed to be allowable for at least the above-identified reasons.

4. Rejection of Claims 1-17 under 35 U.S.C. 103(a)

Claims 1-17 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Hughes, Jr. (U.S. Patent Number 4,493,079; referred to hereinbelow as "Hughes, Jr.") in view of Regelman et al. (U.S. Patent Number 6,574,626; referred to hereinbelow as "Regelman"). Applicants respectfully traverse this rejection.

Claim 1

Claim 1 calls for a machine-executable method comprising reading a test file having a plurality of test vectors; determining a required memory needed to execute the plurality of test vectors; and using the required memory to estimate a cost to execute the test vectors.

With respect to claim 1, the Examiner asserts , in part:

> *...Hughes, Jr. does not disclose determining a required memory needed to execute the plurality of test vectors and using the required memory to estimate a cost to execute the test vectors.*

See, page 4 of the Office Action dated July 31, 2006.

Applicants agree with the Examiner that Hughes, Jr. does not disclose determining a required memory needed to execute the plurality of test vectors and using the required memory to estimate a cost to execute the test vectors.

With respect to claim 1, the Examiner further asserts (underlined emphasis added), in part:

> ..., **Regelman teaches determining a required memory needed to execute the plurality of test vectors (column 2 lines 31-34)**; and using the required memory to estimate a cost to execute the test vectors (*the examiner views this limitation as since the required memory is determined, the estimated cost can be determined. In addition, the estimated cost is determined based on how much memory is required. Since the memory is costly we the public would know that the estimated cost will also be costly.)*

See, page 4 of the Office Action dated July 31, 2006.

Applicants respectfully disagree Regelman does not teach or suggest determining a required memory needed to execute a plurality of test vectors, and using the required memory to estimate a cost to execute the test vectors. At column 2, lines 31-34, Regelman states:

> ...As test programs increase in size, a natural solution is to merely increase the amount of embedded SRAM in order to accommodate the entire test program. SRAM, however, is expensive.

This is merely a general statement of fact that memory is expensive. This fact does not dictate nor suggest a need to *estimate* a cost to execute a plurality of test vectors.

It is further noted that claim 1 recites, in part, determining a required memory needed ***to execute*** the plurality of test vectors; and then using the required memory to estimate a cost ***to execute*** the test vectors." In contrast, Regelman recites, "merely increase[ing] the amount of embedded SRAM in order ***to accommodate*** the entire test program." Regelman fails to teach "using the required memory to estimate a cost ***to execute*** the test vectors", as is recited in Applicants' claim 1.

With respect to claim 1, the Examiner further asserts, in part:

> ... It would have been obvious to one of ordinary skill in the art at the time the invention was made to include determining a required memory and estimated the cost, as disclosed by Regelman, incorporated into Hughes, Jr. so that cost effective memory can be used to satisfy the problem.

See, pages 4 and 5 of the Office Action dated July 31, 2006.

However, as discussed above, Regelman does not teach or suggest determining a required memory needed ***to execute*** the plurality of test vectors, and Regelman does not teach or suggest using the required memory ***to estimate*** a cost to execute the test vectors. Accordingly, claim 1 is believed to be allowable.

Claims 2-7

Claims 2-7, which each depend either directly or ultimately from independent claim 1, are believed to be allowable for at least the above-identified reasons.

Claim 8

Claim 8 calls for system comprising logic to read a test file having a plurality of test vectors and to determine a required memory needed to execute the plurality of test vectors; and a billing predictor, communicatively coupled to the logic, to use the required memory to estimate a cost to execute the test vectors.

The Examiner indicates on page 6 of the Office Action dated July 31, 2006 that claim 8 stands rejected under similar rationale as set for in claim 1.

With respect to claim 8, the Examiner does not specify whether Hughes, Jr. or Regelman teach or suggest a system having logic to read a test file having a plurality of test vectors and to determine a required memory needed to execute the plurality of test vectors. As discussed above, the Examiner states (underlined emphasis added):

> ..., **Regelman teaches determining a required memory needed to execute the plurality of test vectors (column 2 lines 31-34)**; and using the required memory to estimate a cost to execute the test vectors (*the examiner views this limitation as since the required memory is determined, the estimated cost can be determined. In addition, the estimated cost is determined based on how much memory is required. Since the memory is costly we the public would know that the estimated cost will also be costly.)*

See, page 4 of the Office Action dated July 31, 2006.

Applicants respectfully disagree As discussed above with respect to claim 1, Regelman does not teach or suggest determining a required memory needed to execute a plurality of test vectors, and using the required memory to estimate a cost to execute the test vectors. Similarly, and with respect to claim 8,

Regelman does not teach or suggest a system having logic to read a test file having a plurality of test vectors and to determine a required memory needed to execute the plurality of test vectors.

Furthermore, Regelman does not teach, suggest or provide any motivation for a billing predictor, communicatively coupled to the logic, to use a required memory to estimate a cost to execute the test vectors. Accordingly, claim 8 is believed to be allowable.

Claims 9-12

Claims 9-12, which each depend directly from independent claim 8, are believed to be allowable for at least the above-identified reasons.

Claim 13

Claim 13 calls for one or more machine-readable mediums having stored thereon sequences of instructions, which, when executed by a machine, cause the machine to perform the actions: reading a test file having a plurality of test vectors; determining a required memory needed to execute the plurality of test vectors; and using the required memory to estimate a cost to execute the test vectors.

The Examiner indicates on page 6 of the Office Action dated July 31, 2006 that claim 13 stands rejected under similar rationale as set for in claim 1.

With respect to claim 1, and Applicants assume with respect to claim 13 as well, the Examiner asserts (underlined emphasis added), in part:

> ..., **Regelman teaches determining a required memory needed to execute the plurality of test vectors (column 2 lines 31-34)**; and using the required memory to estimate a cost to execute the test vectors (*the examiner views this limitation as since the required memory is determined, the estimated cost can be determined. In addition, the estimated cost is determined based on how much memory is required. Since the memory is costly we the public would know that the estimated cost will also be costly.)*

See, page 4 of the Office Action dated July 31, 2006.

Applicants respectfully disagree Regelman does not teach or suggest determining a required memory needed to execute a plurality of test vectors, and using the required memory to estimate a cost to execute the test vectors. As discussed with respect to claim 1 above, Regelman states:

> ...As test programs increase in size, a natural solution is to merely increase the amount of embedded SRAM in order to accommodate the entire test program. SRAM, however, is expensive.

See, column 2, lines 31-34 of Regelman.

This is merely a general statement of fact that memory is expensive. This fact does not dictate nor suggest a need ***to estimate*** a cost to execute a plurality of test vectors.

It is further noted that claim 13 recites, in part, determining a required memory needed ***to execute*** the plurality of test vectors; and then using the required memory to estimate a cost ***to execute*** the test vectors." In contrast, Regelman recites, "merely increase[ing] the amount of embedded SRAM in order ***to accommodate*** the entire test program." Regelman fails to teach "using the required memory to estimate a cost ***to execute*** the test vectors", as is recited in Applicants' claim 13.

With respect to claim 1, and Applicants assume with respect to claim 13 as well, the Examiner further asserts, in part:

> ... It would have been obvious to one of ordinary skill in the art at the time the invention was made to include determining a required memory and estimated the cost, as disclosed by Regelman, incorporated into Hughes, Jr. so that cost effective memory can be used to satisfy the problem.

See, pages 4 and 5 of the Office Action dated July 31, 2006.

However, as discussed above, Regelman does not teach or suggest determining a required memory needed ***to execute*** the plurality of test vectors, and Regelman does not teach or suggest using the required memory ***to***

estimate a cost to execute the test vectors. Accordingly, claim 13 is believed to be allowable.

Claims 14-17

Claims 14-17, which each depend directly from independent claim 13, are believed to be allowable for at least the above-identified reasons.

5. Conclusion

In light of the amendments and remarks provided herein, Applicants respectfully request the timely issuance of a Notice of Allowance.

Respectfully submitted,
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